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Short communication

Thin and flexible silicon anode based on integrated macroporous silicon film onto electrodeposited copper current collector

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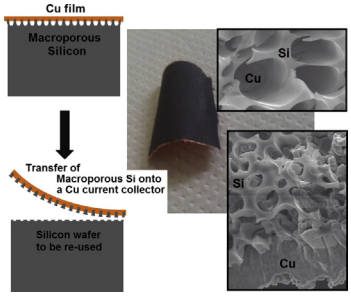
HIGHLIGHTS

- Macroporous silicon is used as negative electrode for lithium-ion batteries.
- A copper current collector is electrodeposited directly on the top of the macropores.
- A self-supported Cu/pSi is obtained with low interface resistance.
- A stable capacity of 1360 mAh g^{-1} in EC/DMC $LiPF_6$ 1 M is achieved at 0.2 A g^{-1}.

GRAPHICAL ABSTRACT



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ABSTRACT

The integration of a macroporous Si (pSi) layer on an electrodeposited Cu current collector is proposed as a facile, low-cost and industrial-scalable procedure to elaborate efficient new anode material for lithium-ion batteries. The preparation process consists of i) formation of macropores on a Si wafer by electrochemical etching, ii) chemical deposition of Cu NPs on microstructured Si, iii) electroplating of a thick continuous Cu film, and iv) peeling of pSi–Cu film. The anode device is flexible and presents a total thickness, comprising the current collector, of 25 μm. SEM characterization shows the partial integration of the copper film inside the Si porous structure. Electrochemical impedance spectroscopy measurements showed this architecture enhances the electrical contact between the Cu current collector and the pSi due to the optimized interface of the two materials. A specific capacity of 1360 mAh g^{-1} in EC/DMC $LiPF_6$ 1 M is achieved at low galvanostatic discharge current (0.2 A g^{-1}). Even during cycling at a high current density of 1.8 A g^{-1}, the macroporous silicon anode was stable, demonstrating a specific capacity of 750 mAh g^{-1} twice as large as graphite based anodes.

1. Introduction

As a trend of challenge, silicon is the main candidate to replace carbon in lithium-ion batteries, due to its much higher theoretical gravimetric capacity of 3600 mAh g^{-1} at room temperature compared to 370 mAh g^{-1} for lithiated graphite (LiC_6) based anode [1]. Because of its strong volume change during lithium insertion

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and de-insertion, bulk single crystalline silicon wafers undergo major crackings and pulverization during cycling, making it unsuitable for a reliable negative electrode material. Nanostructured Si materials that would be stable toward volumetric expansion and shrinking are developed as suitable anode materials. Especially main works focus on the use of silicon nanowires and nanoparticles (NPs) [2–5]. Porous silicon is also investigated as an active material in lithium batteries [6–12]. Due to its morphology, porous Si would be a better way to prepare 3D microbatteries than Si nanowires forest [13]. Nevertheless, one of the issues that porous silicon encounters is the presence of bulk silicon at the bottom of the pores, that promotes cracking and pulverization, similarly to the flat Si wafers (Fig. 1a(*i*)). This issue has been recently skirted by Biswal's group in using macroporous Si (pSi) particles [8] or by Föll's group using optimized array of Si nanowires [14,15]. In this paper, we present an inexpensive and industrially scalable procedure to prepare pSi-based anodes (Fig. 1a(*ii*)). The preparation process of this anode consists of (a) electrochemical etching of a Si wafer to form a pSi layer, (b) growth of a copper-based current collector layer on top, and (c) mechanical peeling off of both layers from the wafer to obtain a free standing film with an optimized interfacial resistance between the metallic collector and the anode material. Morphological characterizations of the pSi surface is achieved by scanning electron microscopy (SEM), and electrochemical characterizations are performed using cyclic voltammetry (CV), galvanostatic cycling and electrochemical impedance spectroscopy (EIS).

2. Experimental

2.1. Preparation of macroporous silicon

The pSi layer was prepared in a 5 wt. % HF/H_2O acid electrolyte added with 350 ppm Cetyltrimethylammonium Chloride (CTAC) surfactant from Aldrich®. The silicon wafer is p-type doped with a 30–50 Ω cm resistivity and a (100) crystalline orientation. The pSi etching was performed in a double tank electrochemical cell. The anodic polarization of the wafer is assumed by a backside electrolytic contact. This electrolytic contact and the p^+ doping of the wafer backside ensure a homogeneous potential distribution. To achieve the macroporous layer, a 10 mA cm^{-2} current density was applied during 90 min.

2.2. Transfer of macroporous silicon layer on copper current collector

Native oxide formed on pSi wafer chip of 9 cm^2 was chemically etched by soaking in an aqueous fluoride solution (2.5% hydrofluoric acid) for 90 s. Before the Cu electroplating on the pSi, an intermediary stage is achieved, consisting in a copper seeding procedure using an electroless deposition of Cu NPs following the reactions described in Ref. [14]. This Cu seeding is to ensure a good electrical contact between Si and Cu current collector. The freshly etched sample was transferred into an aqueous fluoride solution

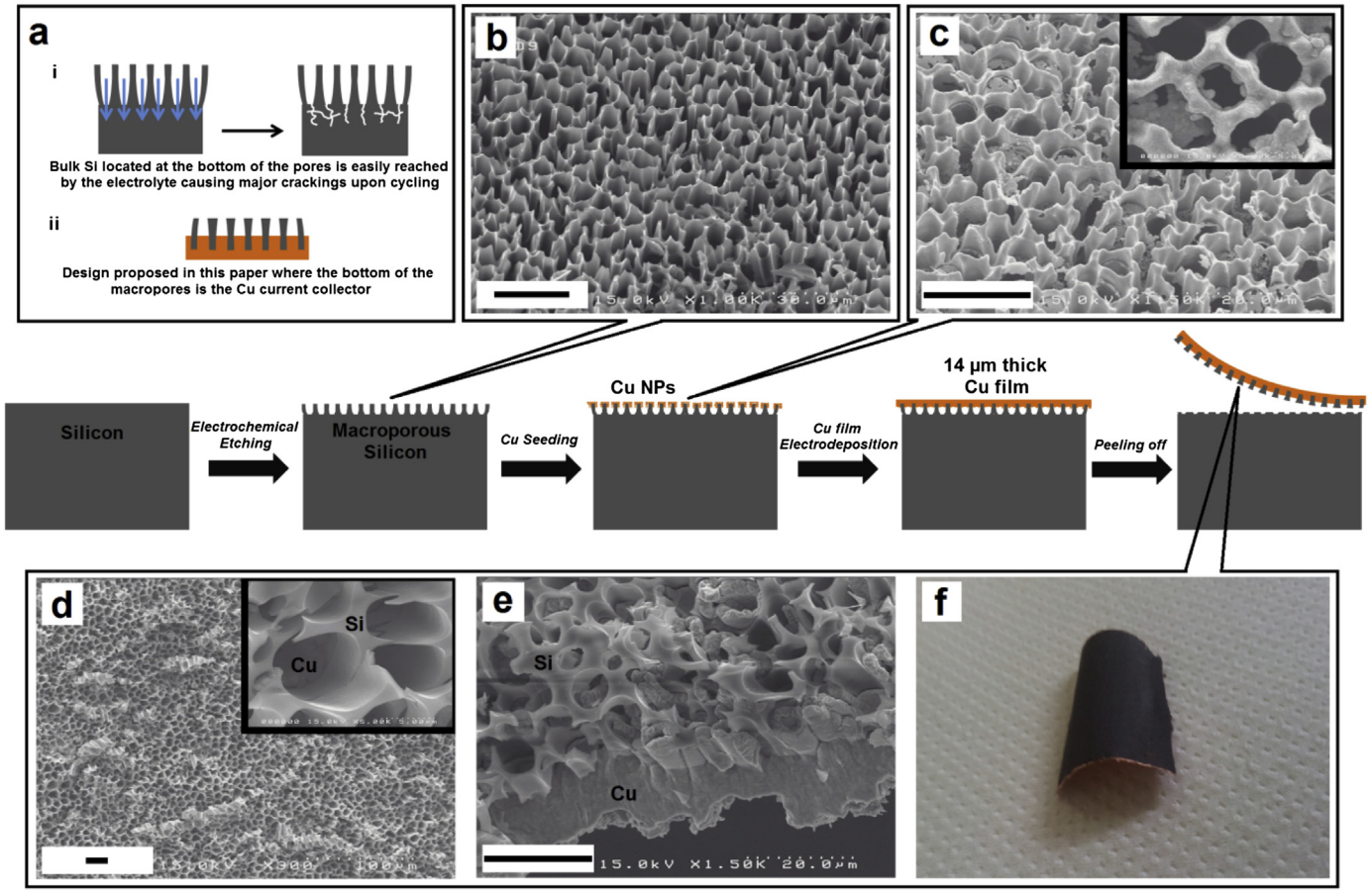

Fig. 1. Strategy used for integrating a pSi layer on an electrodeposited copper current collector. (a) Schematic representation of (*i*) cracking issue due to the presence of bulk Si underneath, and (*ii*) how it is solved in this study. (b) SEM image of a pSi wafer (Tilted view). (c) SEM image of the pSi wafer covered by Cu NPs (Tilted view). Inset: Higher magnification. (d) SEM image of a peeled pSi–Cu film. Inset: Higher magnification. (e) SEM image of the edge of pSi–Cu film. (f) Photograph of the pSi–Cu film. All scale bars in SEM images represent 20 μm.

(0.8% hydrofluoric acid) containing 90 mM of $CuSO_4$ ($CuSO_4 \cdot 5H_2O$, Fisher®) for 300 s at room temperature. This Cu thin film on microstructured Si serves as a bedrock for the thick continuous electrodeposited Cu film. After thoroughly washing with deionized water, the sample was placed in a three electrodes electrochemical cell where the Si wafer, a platinum wire, and a platinum foil acted as the working electrode, the pseudo-reference electrode, and the auxiliary electrode, respectively. The copper electroplating solution was composed with 10 mM $CuSO_4$ and 1.8 M H_2SO_4 (H_2SO_4 98%, Alfa Aesar®). The current density for the Cu deposition was fixed at 1 mA cm^{-2} and held for 20 h at room temperature. Once the electroplating of copper was finished reaching the electrodeposition of about 240 mg of Cu, the sample was copiously rinsed with deionized water and then blown dry under nitrogen. The last step consisted of mechanically peeling off the Cu film from the Si wafer. The Cu layer was peeled off manually from the wafer, with the most part of pSi layer following to it. Before storing in a glovebox, pSi–Cu films were finally dried at 65 °C under vacuum for 48 h.

2.3. Characterizations

Electrochemical half-cells were prepared in an argon-filled glovebox (water and dioxygen contents below 10 ppm) within the form of 2032 two electrodes coin cells where the working electrodes were dried pSi–Cu films and the counter electrodes were lithium foils. The working and the counter electrodes were separated with a polypropylene membrane (Celgard® 2400) and a glass microfiber membrane (Whatman® GF/C) impregnated with 1 M $LiPF_6$ dissolved in a 1:1 (v/v) mixture of ethylene carbonate (EC, Sigma–Aldrich®) and dimethylcarbonate (DMC, Sigma–Aldrich®). Cyclic voltammograms (CVs) were recorded at a scan rate of 0.1 mV s^{-1} between 0.02 and 2 V versus Li/Li^+. Galvanostatic cycling was performed at different current densities with two different potential limits cut-off, between 0.02 and 2 V or between 0.125 and 0.7 V. All impedance measurements were performed at the open circuit voltage of the electrochemical cell between 1 MHz and 100 mHz with signal amplitude of 7 mV. All electrochemical measurements were made with a Biologic® VMP3. SEM images were observed with a Hitachi 4600 scanning electron microscope at an accelerating voltage of 15 kV.

3. Results and discussion

The electrochemical etching of the silicon wafer achieves macropores (Fig. 1b) with a depth of 17 μm and a diameter range of 5–8 μm. The formation of Cu NPs is fast and a reaction time of 300 s resulted in a Cu NPs layer of about 300 nm-thick (Fig. 1c). The electroless deposition of this homogeneous Cu NPs layer occurs essentially on the top of the macrostructured Si, whereas few or no NPs have been observed at the bottom of the pores (inset of Fig. 1c). SEM observation after peeling shows that the obtained pSi–Cu film surface is homogeneous (Fig. 1d) and at higher magnification it is possible to descry the Cu seeding film at the bottom of the macropores (inset of Fig. 1d). A cross sectional view (Fig. 1e) shows that the electrodeposited Cu film can penetrate inside some of the pores, which is beneficial for a good electrical contact between the Si material and the Cu current collector. Nevertheless, the porous structure is still present (in one side of the porous film) which means that the pores are not totally filled with the copper. The thickness of the copper film electrodeposited on the top of the macropores substrate is around 14 μm. Peeling off does not require special precaution, as the Cu layer is robust enough. The Si mass peeled off from the wafer is determined from SEM observations. In considering an average thickness of the macroporous film of 10.4 μm (from an initial pSi thickness of 17 μm) and an average pore diameter of 7.2 μm, the mass of Si is estimated to 0.55 mg cm^{-2}. Only the mass of Si serves to determine capacities. The photograph of the final device (Fig. 1f) shows, at a macroscopic scale, the homogeneity of the integrated pSi on the Cu current collector and the flexibility of the pSi–Cu film. The use of porous silicon instead of bare silicon increase the interface between the electrolyte and the active material. For a given apparent surface of 0.5 cm^2, the real surface is largely increased which allow to increase the charge–discharge gravimetric current without strong decrease of the specific capacity. Moreover, the integration of current collector inside the porous silicon film as a self-supported pSi/Cu materials should improve the interface resistance of the nanocomposite and decrease the ohmic drop for high discharge currents.

Fig. 2 shows CVs performed in EC/DMC containing 1 M $LiPF_6$ between 0.02 and 2 V vs Li/Li^+ at a scan rate of 0.1 mV s^{-1}. The inset of Fig. 2 displays the potential region where irreversible reactions occur. These cathodic reactions are mainly observable on the first cycle where the cathodic peaks are located at 1.6, 1.2 and 0.7 V versus Li/Li^+. The two first waves would be attributed to the reduction of adventitious contaminations, or water traces or silicon oxide species [16–18]. The third cathodic peak at the lowest potential would correspond to the irreversible electrolyte reduction and the solid electrolyte interface (SEI) formation [18,19]. It is worth noting that the two first peaks are totally suppressed on the four consecutive scans whereas the third peak attributed to the SEI formation remains, with lower peak intensity though. This finding could be explained by a partial solubilization of the SEI layer and its re-deposition on the electrode after later reduction. Fig. 2 also displays the CVs from the 2nd to the 50th scans. The second scan shows a broad cathodic peak at 0.16 V with a shouldering peak at 0.24 V, corresponding to the lithiation of the porous Si on two different Si microstructures. The lithiation process would occur here on an amorphous Si and crystalline Si. Indeed during the first cycle, a part of the Si volume is affected by the lithiation, and this part is then delithiated on the reverse scan forming amorphous Si. Thus, in the second cycle, there exist two microstructures, the amorphous Si phase and the remaining crystalline part of Si not previously affected by the first cycle [10,12,20,21]. On the reverse scan, anodic peaks located at potentials of 0.32 and 0.52 V would be attributed to the delithiation reaction of Li–Si phases [10–12]. Anodic peak at 0.9 V may be also attributed to phase transition of lithiated silicon alloy [12]. The 50th curve is superimposed on the 40th, whereas from the 2nd to the 40th scan, the intensity of both anodic and cathodic peaks increases. Monitoring this intensity

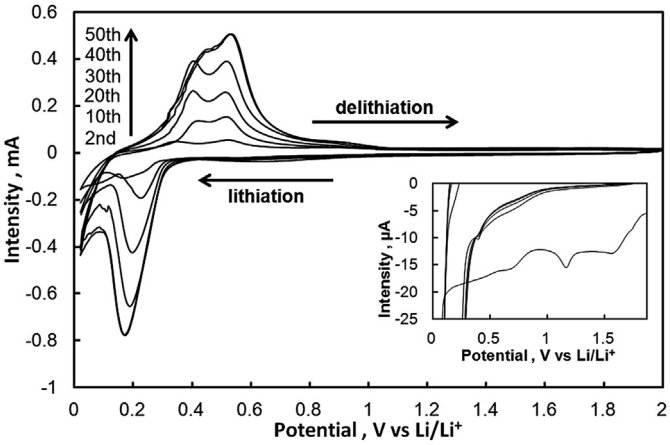

Fig. 2. Cyclic voltammograms of a pSi–Cu anode in EC/DMC + $LiPF_6$ at a scan rate of 0.1 mV s^{-1}.

increase would demonstrate that lithiation and delithiation reactions are controlled by the Li incorporation in the thickness of the Si film. As far as the CVs are recorded to the 40th scan, the Li penetrates deeper in the porous walls, raising the peaks intensity and the polarization. We observed no current intensity decrease even for 50 consecutive voltammogram cycles. This information is crucial for showing no material loss during this long time experiment.

Galvanostatic cycling was first performed at a current density of 0.2 A g^{-1} (C/20) with limit cut-off potentials of 0.05 V and 2 V (Fig. 3a). The initial insertion capacity was 1750 mAh g^{-1}. A heavy decrease of the capacity occurs for a decade of cycles. Insertion/deinsertion cycles were then run at a lower rate, 0.1 A g^{-1} (C/40), and we observed that the insertion capacity recovered 1380 mAh g^{-1} which is 6 times as large as the last capacity value obtained from the last charge–discharge cycle at a rate of 0.2 A g^{-1} (C/20). This would mean that the strong fading observed is principally due to the evolution of the thickness of the SEI film on the pSi anode during cycling rather than an irreversible loss of the electrochemical activity of the pSi material. Differential capacity curves (Fig. 3b) clearly show the electrolyte decomposition during discharging and this cathodic peak (0.52 V vs Li/Li^+) attributed to the formation of the SEI remains over cycling. This observation would signify that a continuously growing SEI is formed getting thicker through the duration of the galvanostatic measurements. It is known that cycling in a wide potential window, from 0.05 to 2 V, promotes strong interfacial changes for a Si-based anode [19]. Cui's group showed that limiting the cut-off voltage is an effective way in suppression of morphological change in SEI and thus in improvement of the capacity retention. They demonstrated that the SEI is continuously growing even in the low potential window, e.g. lower than the potential determined by CV where the SEI forms, showing that Si nanowires are far more coated by the SEI when cycling to 0.01 V than cycling to 0.1 V [19]. For potential limits from 0.125 to 0.7 V (Fig. 4a), we effectively observed that galvanostatic cycles show a stable behavior at a current density of 0.2 A g^{-1} (C/20). The first cycle leads to discharge capacity of 1350 mAh g^{-1}. After a decade of cycles, a perceptible gain in capacity is obtained with a value about 1% (Fig. 4a). At higher current densities, 0.4, 0.7 and 1.8 A g^{-1} (respectively C/10, C/5 and C/2), stable capacities are recorded with respective values of 1200, 1000 and 750 mAh g^{-1}. A strong decrease is observed for an applied current density of 3.6 A g^{-1}. This behavior at the highest rate may be due to the limitation of solid-state ion diffusion in the Si that cannot permit Li to alloy the Si material in depth [10]. This apparent fading is not due to a loss or degradation of the material as the capacity returns to its precedent value at a lower rate of 1.8 A g^{-1}. Here, differential capacity curves displayed in Fig. 4b show for the first discharge that a cathodic peak is present at 0.52 V vs Li/Li^+, attributed to the electrolyte decomposition and the SEI formation. For subsequent cycles, this peak disappears signifying that the formation of the SEI would be limited. Therefore, cycling in limiting the potential cut-offs would permit to lower the morphological changes of the SEI, and additionally limiting the lower cut-off potential to 0.125 V would limit the Si volume expansion. Controlling these parameters would enhance the capacity retention.

Electrochemical impedance studies were performed after 10 galvanostatic cycles for potential limitations between 0.05 and 2 V

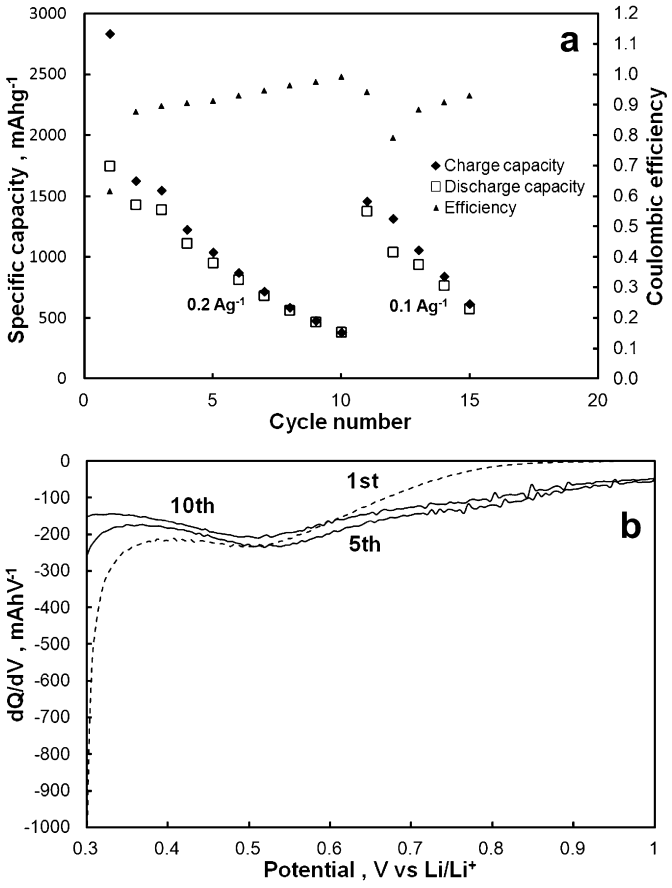

Fig. 3. (a) Galvanostatic profiles for a Li/pSi–Cu half-cell with voltage cutoffs of 0.05 V and 2 V. (b) Differential capacity curves for a Li/pSi–Cu half-cell with voltage cutoffs of 0.05 V and 2 V.

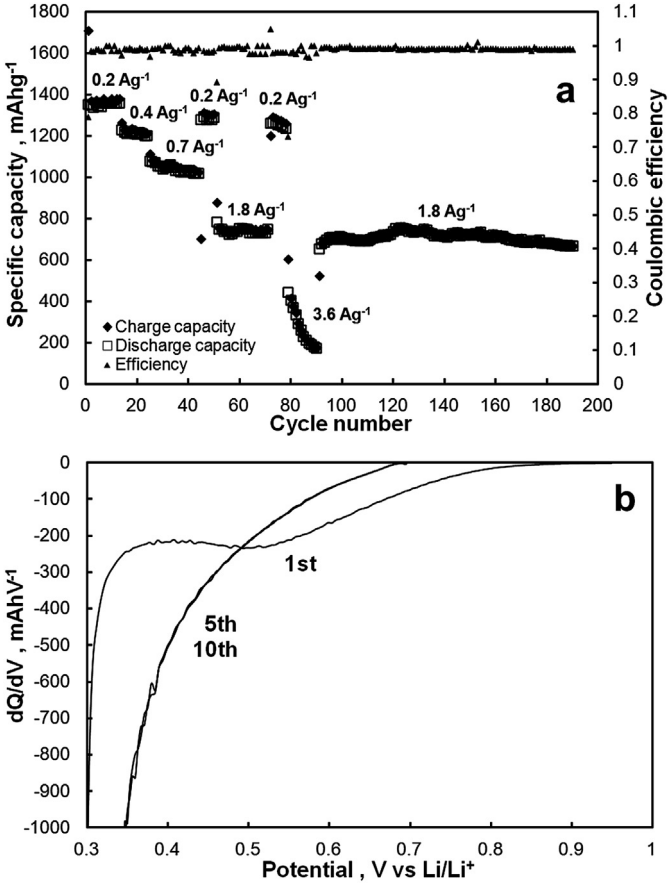

Fig. 4. (a) Galvanostatic profiles for a Li/pSi–Cu half-cell with voltage cutoffs of 0.125 V and 0.7 V. (b) Differential capacity curves for a Li/pSi–Cu half-cell with voltage cutoffs of 0.125 V and 0.7 V.

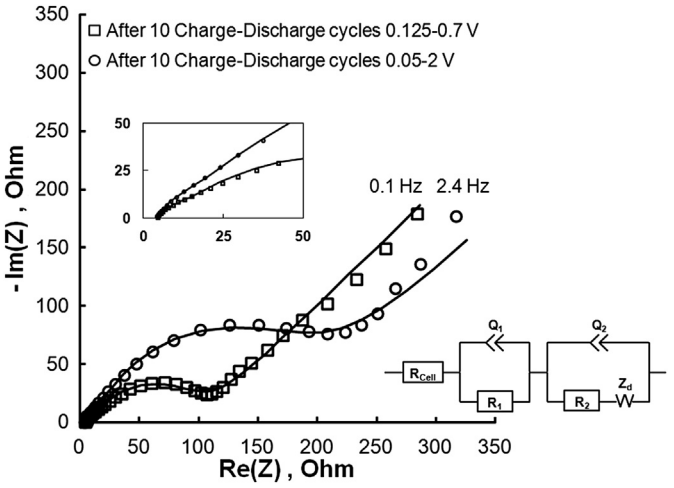

Fig. 5. Nyquist diagrams of the Li/pSi–Cu half-cells recorded after 10 charge–discharge cycles achieved for different cutoffs voltage.

and after 10 galvanostatic cycles for potential limitations between 0.125 and 0.7 V. Total impedance of the Li/electrolyte/pSi system is displayed as Nyquist diagrams in Fig. 5. In both cases, suppressed semi-circles in the high frequencies are present whereas at low frequencies the diagrams show a straight line. These Nyquist diagrams are modeled with the equivalent electrical circuit (inset of Fig. 5). R_{cell} represents the electrolyte solution resistance, C_1 and R_1 are respectively the pseudocapacitance and resistance both associated to the Si/Cu interface, C_2 and R_2 are respectively the double layer pseudocapacitance and the resistance associated to the ionic migration inside the SEI and to the charge transfer resistance at the Si/SEI interface and finally Z_d is the Warburg element. The values of C_1 and R_1 deduced from fitting to two Nyquist diagrams are very similar, $C_1 = 2$ μF and $R_1 = 7.5$ Ω, meaning that the fading observed during the galvanostatic cycling in the larger potential window is not due to the alteration of the Si/Cu interface. Two phenomena may affect the diameter of second suppressed semi-circle, which is assigned to the electrolyte/Si interface: the formation of SEI and the volume expansion of Si. A thicker SEI layer would bring about a larger diameter of the semi-circle, because its ionic conductivity would be restricted. On the other hand, a larger volume of Si would enhance its specific area and should be accompanied by an increase of the ionic conductivity and a diminishing of the charge transfer resistance, leading to a smaller diameter of the semi-circle. Here we observed a larger semi-circle when the cut-off potentials are from 0.05 to 2 V, with $R_2 = 193$ Ω compared to a R_2 value of 92 Ω when the cut-off potentials are from 0.125 to 0.7 V. We, therefore, suppose that the major phenomena affecting the impedance of the system is the formation of a thicker SEI caused by larger potential windows. At low frequencies, the impedance of the ions diffusion is lowered for the sample cycled in a limited potential window, indicating that, in this case, the SEI is more favorable to the conduction of ions. Such observations based on the description of the Nyquist diagrams suggest that the formation of SEI is essential for improving the cycling properties of our system.

4. Conclusion

Silicon-based flexible negative electrodes of a new design were achieved from a macroporous silicon wafer. The preparation process consists of i) formation of macropores on a Si wafer by electrochemical etching, ii) chemical deposition of Cu NPs on microstructured Si, iii) electroplating of a thick continuous Cu film, and iv) peeling of pSi–Cu film. This procedure is low cost (inexpensive materials, reusability of the wafer) and low time-consuming and, therefore, is industrial friendly. Galvanostatic cycling in a wide range of potential, between 0.05 and 2 V, induced the formation of a thick SEI, and a fast fading of the capacity. However, by reducing the voltage range, between 0.125 and 0.7 V, stable and high capacities have been reached. The specific capacity is 1360 mAh g^{-1} at a rate of 0.2 A g^{-1}, while it is 750 mAh g^{-1} at high current density of 1.8 A g^{-1}.

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